What Is Claimed Is:

1. A method for performing a two-dimensional (2D) inverse discrete cosine transform (IDCT) on a series of 2D-transform coefficient blocks, wherein the method comprises:

receiving multiple coefficient blocks from the series of 2D-transform coefficient blocks;

grouping together a respective element from each of the multiple coefficient blocks to produce one block of 2D coefficient vectors; and

operating on the block of 2D coefficient vectors with SIMD instructions to carry out the 2D-IDCT on the multiple coefficient blocks.

2. The method of claim 1, wherein the SIMD instructions are floating point instructions.

3. The method of claim 1, wherein the multiple coefficient blocks consist of exactly two coefficient blocks at a time.

4. The method of claim 1, wherein the operating includes:

carrying out a one-dimensional (1D) IDCT on each row of 2D coefficient vectors with SIMD instructions to produce a block of 1D transform coefficient vectors;

carrying out a 1D-IDCT on each column of 1D transform coefficient vectors with SIMD instructions to produce inverse-transformed data value vectors.

5. The method of claim 4, further comprising:

isolating and arranging elements of the inverse-transformed data value vectors to form multiple inverse-transformed data blocks that correspond to the multiple coefficient blocks.

6. An information carrier medium configured to convey software to a general purpose computer system that supports SIMD instructions, wherein the software comprises a two-dimensional (2D) inverse discrete cosine transform (IDCT) module having:

an input interface configured to receive multiple two-dimensional discrete cosine transform (2D-DCT) coefficient blocks;

a first set of instruction code configured to collect and assemble respective coefficients from the multiple 2D-IDCT coefficient blocks to form coefficient vectors having one coefficient from each of the 2D-IDCT coefficient blocks, wherein the relationship between the coefficients of the coefficient vectors, once established, is maintained unaltered in the transform module;

SIMD instructions configured to operate on the coefficient vectors to carry out a 2D-IDCT of the multiple coefficient blocks in parallel; and

a second set of instruction code configured to extract and arrange inverse-transformed elements of the coefficient vectors to produce multiple inverse-transformed data blocks corresponding to the received multiple 2D-DCT coefficient blocks.

7. The medium of claim 6, wherein the SIMD instructions include:

a first set of SIMD instructions to perform an IDCT on each row of the coefficient vectors to produce one-dimensional (1D) DCT coefficient vectors; and

a second set of SIMD instructions to perform an IDCT on each column of the 1D-DCT coefficient vectors to produce inverse transformed data vectors.

8. The medium of claim 6, wherein the multiple 2D-DCT coefficient blocks consist of exactly two 2D-DCT coefficient blocks.

9. The medium of claim 6, wherein the SIMD instructions include floating point instructions.

10. The medium of claim 6, wherein the medium is a digital information storage medium that is one of a set consisting of: printed paper, punched paper, magnetic tape, magnetic disk, optical disk, redundant array of independent disks, non-volatile memory array, and volatile memory array.

11. The medium of claim 6, wherein the medium is an information transmission medium that is one of a set consisting of: a phone line, a television cable, a wireless link, a satellite link and the Internet.

12. A computer that comprises:

memory storing application software and multimedia data; and

a processor that implements a floating point SIMD instruction set, wherein the processor is coupled to the memory and configured to execute the application software,

wherein the application software includes:

a first module which configures the processor to receive multiple blocks of 2D-DCT coefficients;

a second module which configures the processor to inverse transform the multiple blocks of 2D-DCT coefficients in parallel, wherein the second module includes:

a first set of instruction code that configures the processor to collect respective elements from each of the multiple blocks and to assemble the respective

elements in a plurality of registers so that each register has a single element from each of the multiple blocks;

a first set of SIMD floating point instructions that operate on the register contents to produce 1D-DCT coefficients of the multiple blocks, wherein each of the plurality of registers has a single 1D-DCT coefficient from each of the multiple blocks;

a second set of SIMD floating point instructions that operate on the register contents to produce inverse transformed coefficients of the multiple blocks, wherein each of the plurality of registers has a single inverse transformed coefficient from each of the multiple blocks; and

a second set of instruction code that configures the processor to isolate and arrange the inverse transformed coefficients to form multiple multimedia data blocks that correspond to the originally received multiple blocks.

13. The computer of claim 12, wherein the multiple blocks of 2D-DCT coefficients consist of exactly two blocks.

14. The computer of claim 13, wherein one of the multiple blocks is an all-zero block.